

What is claimed is:

- 1 1. A structure, comprising:
2 a plurality of patterned, spaced apart, substantially co-planar, conductive
3 lines;
4 wherein a first portion of the plurality of conductive lines have a first
5 dielectric of a first dielectric constant therebetween, and a second portion of the
6 plurality of conductive lines have a second dielectric of a second dielectric
7 constant therebetween.
- 1 2. The structure of Claim 1, wherein the first dielectric constant is less than
2 the second dielectric constant.
- 1 3. The structure of Claim 2, wherein the conductive lines comprise a metal
- 1 4. The structure of Claim 3, wherein the metal is selected from the group
2 consisting of aluminum, copper, alloys of aluminum, alloys of copper, titanium,
3 tantalum, tungsten, and nickel.
- 1 5. The structure of Claim 2, wherein the first dielectric comprises an organic
2 polymer.
- 1 6. The structure of Claim 2, wherein the first dielectric comprises a silicon
2 based insulator containing an organic polymer.

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1 7. The structure of Claim 2, wherein the first dielectric comprises a
2 nanofoam.

1 8. The structure of Claim 2, wherein the first dielectric comprises a fluorine
2 doped oxide of silicon.

1 9. The structure of Claim 2, wherein the second dielectric comprises a
2 material having a dielectric constant greater than the dielectric constant of silicon
3 dioxide.

1 10. The structure of Claim 2, wherein the second dielectric comprises barium
2 strontium titanate.

1 11. The structure of Claim 2, wherein at least one of the first portion of the
2 plurality of conductive lines is coupled to a first power supply node, and at least
3 one of the first portion of the plurality of conductive lines is coupled to a second
4 power supply node.

1 12. The structure of Claim 2, wherein at least one of the second portion of the
2 plurality of conductive lines is coupled to a first signal node, and at least one of
3 the second portion of the plurality of conductive lines is coupled to a second
4 signal node.

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1 13. An integrated circuit comprising:
2 a first and a second interconnect line, and a first dielectric material having
3 a first dielectric constant disposed therebetween;
4 a third and a fourth interconnect line and a second dielectric material
5 having a second dielectric constant disposed therebetween;
6 wherein the first and second interconnect lines are coupled to a first and a
7 second power supply node respectively; the third and fourth interconnect lines
8 are coupled to a first and a second signal node respectively; the first, second,
9 third and fourth interconnect lines are on the same interconnect level, and the
10 second dielectric constant is less than the first dielectric constant.

1 14. The integrated circuit of Claim 13, wherein the second dielectric material
2 comprises an organic polymer.

1 15. The microelectronic structure of Claim 13, wherein the second dielectric
2 material comprises a silicon based insulator containing an organic polymer.

1 16. The microelectronic structure of Claim 13, wherein the first dielectric
2 material comprises barium strontium titanate.

1 17. A method of forming an interconnect structure, comprising:
2 forming a first layer of a first dielectric material on a substrate;

3 patterning the first layer;
4 depositing conductive material over the patterned first layer;
5 planarizing the conductive material such that a plurality of interconnect
6 lines are formed;
7 forming a mask layer over the interconnect lines and patterned first layer;
8 patterning the mask layer such that a first portion of the interconnect lines
9 and patterned first layer are covered, and a second portion of the interconnect
10 lines and patterned first layer are uncovered;
11 removing the dielectric material from the uncovered portion;
12 removing the patterned mask layer; and
13 depositing a second layer of a second dielectric material.

1 18. The method of Claim 17, wherein the first dielectric material has a
2 dielectric constant greater than a dielectric constant of the second dielectric
3 material.

1 19. The method of Claim 17, wherein the first dielectric material has a
2 dielectric constant less than a dielectric constant of the second dielectric
3 material.

1 20. A method of forming an interconnect structure, comprising:
2 forming a first layer of a conductive material on a substrate;
3 forming interconnect lines from the conductive material;

4 depositing a first dielectric material over and between the interconnect
5 lines;
6 forming a mask layer over the interconnect lines and first dielectric
7 material;
8 patterning the mask layer such that a first portion of the interconnect lines
9 and first dielectric material are covered, and a second portion of the interconnect
10 lines and first dielectric material are uncovered;
11 removing the first dielectric material from the uncovered portion;
12 removing the patterned mask layer; and
13 depositing a second dielectric material.

1 21. The method of Claim 21, wherein the first dielectric material has a
2 dielectric constant greater than a dielectric constant of the second dielectric
3 material.

1 22. The method of Claim 21, wherein the first dielectric material has a
2 dielectric constant less than a dielectric constant of the second dielectric
3 material.

1 23. A method of making in-plane decoupling capacitors, comprising:
2 forming a first plurality of conductive lines on an insulating substrate, the
3 first plurality of conductive lines having a first dielectric therebetween; and

4 forming a second plurality of conductive lines on the insulating substrate,
5 the second plurality of conductive lines having a second dielectric therebetween;
6 wherein the first dielectric has a dielectric constant greater than a
7 dielectric constant of the second dielectric.

1 24. A method of forming an interconnect structure, comprising:
2 forming, on a substrate, a first plurality of interconnect lines and a first
3 intralayer dielectric disposed between the first plurality of interconnect lines;
4 removing a portion of the first intralayer dielectric;
5 forming a second intralayer dielectric on the substrate where the first
6 intralayer dielectric was removed; and
7 forming a second plurality of interconnect lines in the second intralayer
8 dielectric.

1 25. The method of Claim 24, wherein a dielectric constant of the first
2 intralayer dielectric is different from a dielectric constant of the second intralayer
3 dielectric.

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1 26. The method of Claim 25, wherein forming the second plurality of
2 interconnect lines comprises etching trenches in the second intralayer dielectric,
3 depositing a conductive material, and polishing the conductive material such that
4 the conductive material is substantially removed except for that which is in the
5 trenches.

- 1 27. A method of forming an interconnect structure, comprising:
2 forming a first dielectric layer on a substrate;
3 removing a portion of the first dielectric layer;
4 forming a second dielectric layer on the substrate where the portion of the
5 first dielectric layer was removed; and
6 forming a plurality of interconnect lines in the first and second dielectric
7 layers.

- 1 28. The method of Claim 27, wherein a dielectric constant of the first dielectric
2 is different from a dielectric constant of the second dielectric.

- 1 29. The method of Claim 28, wherein forming the plurality of interconnect
2 lines comprises etching trenches in the first and the second dielectrics,
3 depositing a conductive material, and polishing the conductive material such that
4 the conductive material is substantially removed except for that which is in the
5 trenches.